



HARDWARE

REFERENCE DESIGN

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UM680A

Automotive Grade GNSS High Precision
RTK Positioning Module

Revision History

Version	Revision History	Date
R1.0	First release	Oct. 2024

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Foreword

This document describes the hardware reference design of Unicore UM680A module.

Target Readers

This document applies to technicians who are familiar with GNSS receivers.

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1 Block Diagram

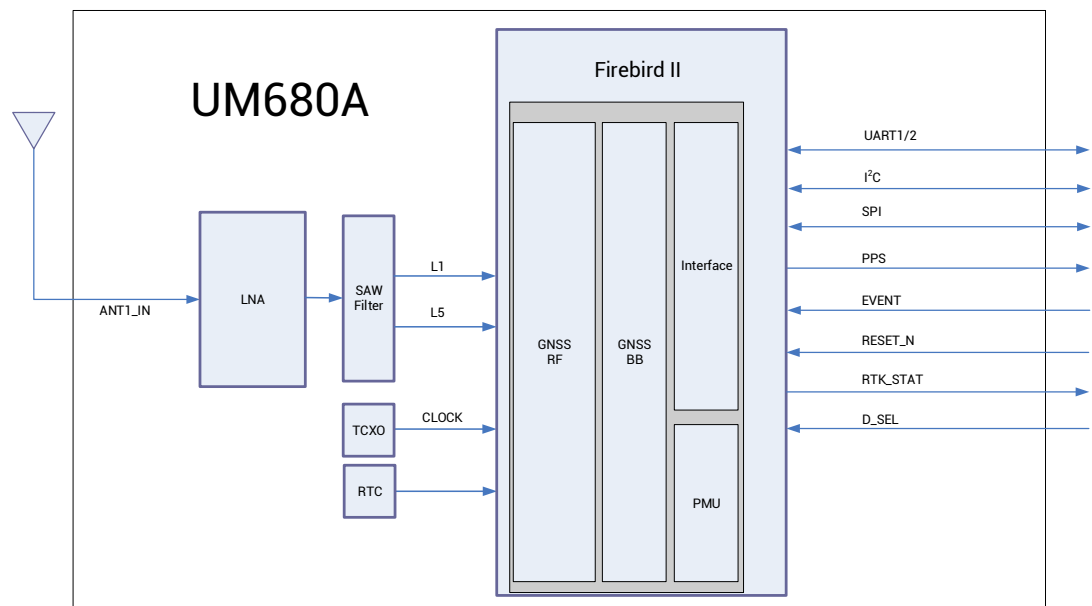


Figure 1-1 UM680A Block Diagram¹

¹ SPI and I²C are reserved interfaces.

2 UM680A Peripheral Design

- Connect the ANT_IN signal to the antenna, and note the 50 Ω impedance matching.
- Connect all the GND pins to the ground.
- Leave the IO pin open if not used.
- Recommended to add TVS anti-surge protection at the input of the module. Add ESD protection at all the used pins.

UM680A Hardware Reference Design

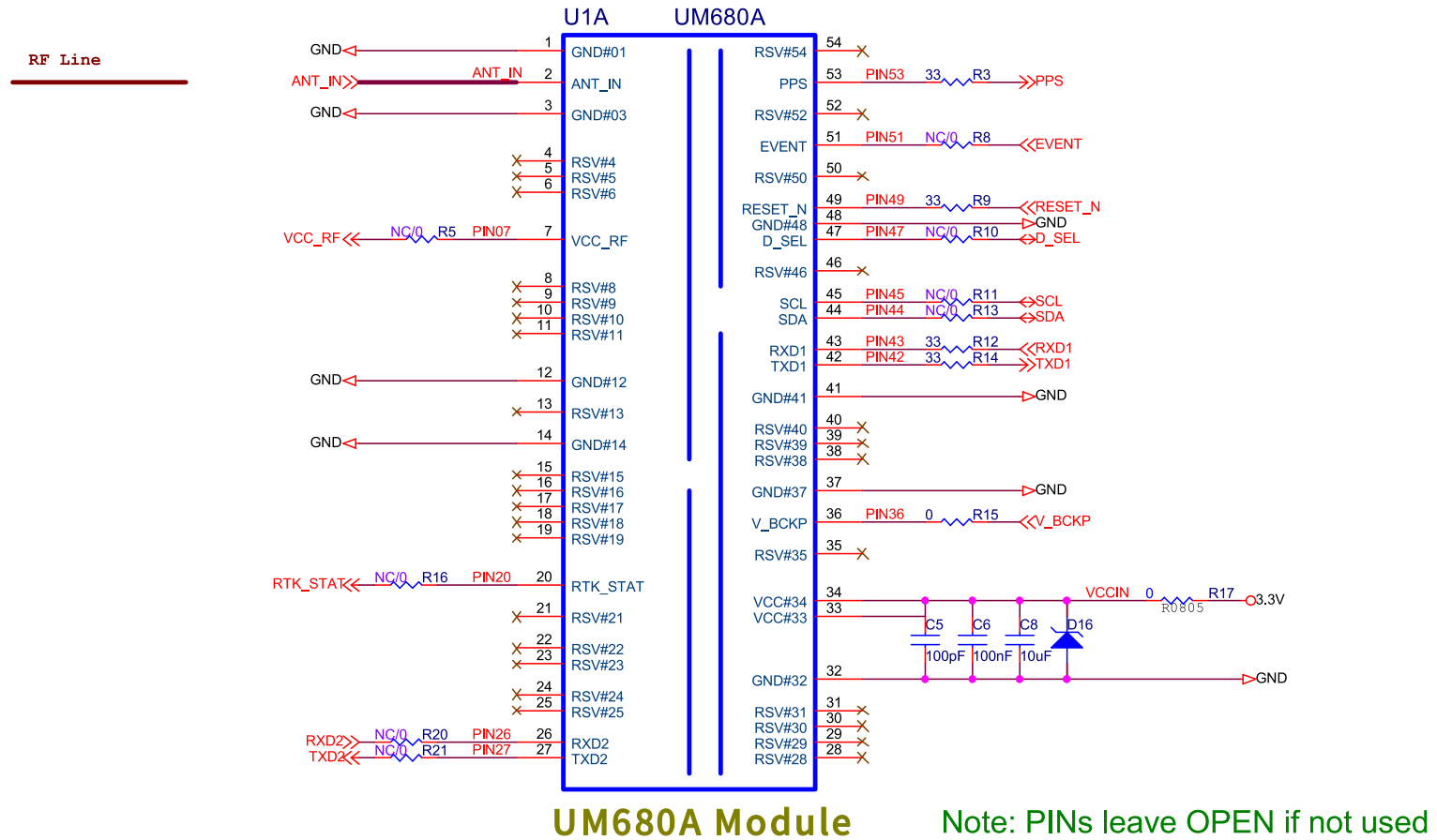


Figure 2-1 UM680A Peripheral Design

The GND pads at the bottom of the module should be grounded to ensure heat dissipation.

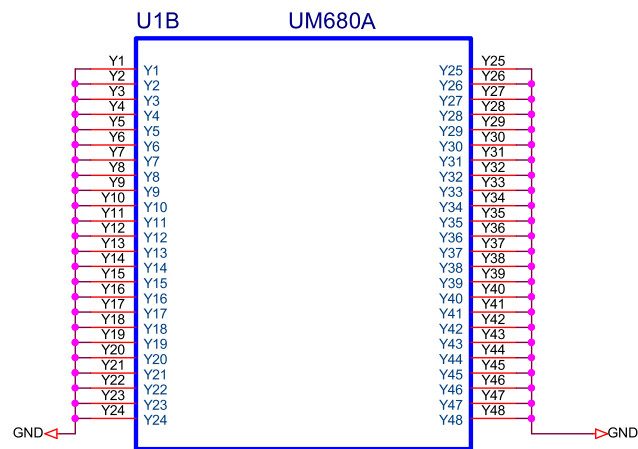


Figure 2-2 UM680A GND Pads

2.1 Main Power VCC

The working voltage range of the module UM680A is 2.7 V to 3.6 V.

Note:

- The VCC initial level when power-on should be less than 0.4 V.
- The VCC ramp when power-on should be monotonic, without plateaus.
- The voltages of undershoot and ringing should be within 5% VCC.
- VCC power-on waveform: The time interval from 10% rising to 90% must be within 100 μ s to 10 ms.
- Power-on time interval: The time interval between the power-off ($V_{CC} < 0.4$ V) to the next power-on must be larger than 500 ms.

2.2 Backup Power V_BCKP

When using the hot start function of the module UM680A, you need to provide backup power for the module. The input range of V_BCKP is 2.0 V to 3.6 V.

Note:

- The V_BCKP initial level when power-on should be less than 0.4 V.
- The V_BCKP ramp when power-on should be monotonic, without plateaus.
- The voltages of undershoot and ringing should be within 5% V_BCKP.
- V_BCKP power-on waveform: The time interval from 10% rising to 90% must be within 100 μ s to 10 ms.
- Power-on time interval: The time interval between the power-off ($V_{BCKP} < 0.4$ V) to the next power-on must be larger than 500 ms.
- When you do not use the hot start function, connect V_BCKP to VCC or a standalone power source. Do not connect it to ground or leave it floating.

2.3 Active Antenna Feed Circuit

The antenna feed circuit consists of the anti-surge design, filter inductors, and ESD protection. The ESD protection diode should support high-frequency signals (above 2000 MHz).

- ✎ It is not recommended to use VCC_RF to feed the antenna, as it has not been optimized for the anti-lightning strike and anti-surge due to the compact size of the module.
- ✎ If the antenna feed supply ANT_BIAS and the module's main supply VCC use the same power rail, the ESD, surge and overvoltage from the antenna will have an effect on VCC, which may cause damage to the module. Therefore, it is recommended to design an independent power rail for the ANT_BIAS to reduce the possibility of module damage.

Connect the ANT_IN signal to the antenna, and note the 50 Ω impedance matching.

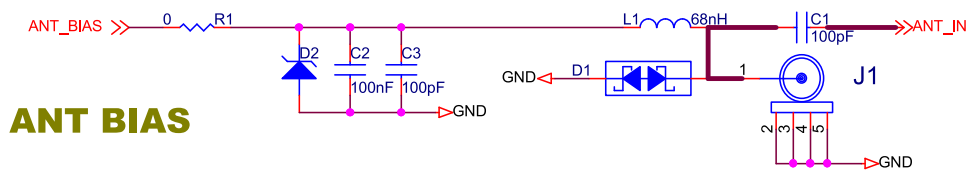


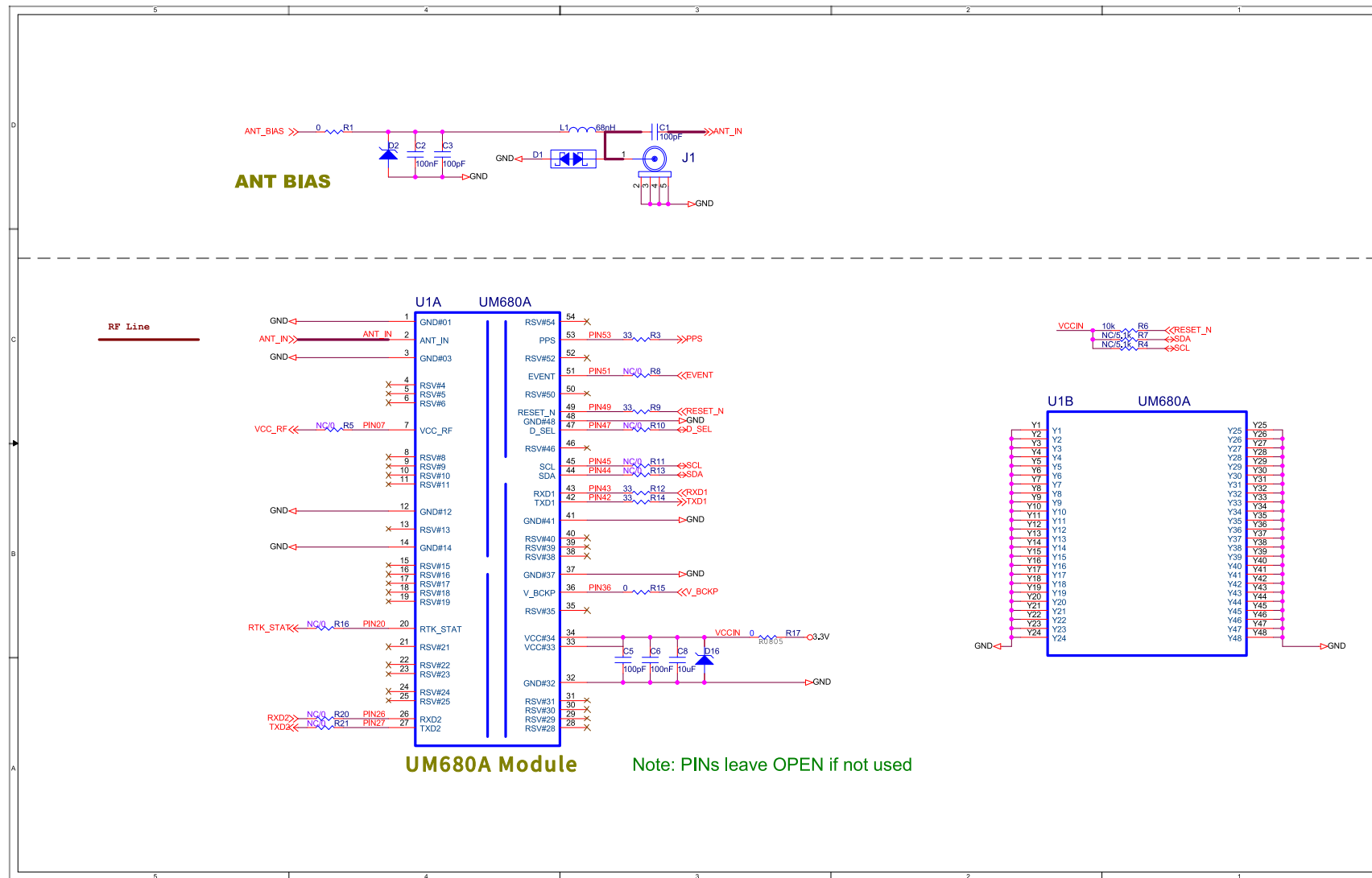
Figure 2-3 Antenna Feed Circuit

2.4 Reset Circuit

UM680A supports system reset. The pin RESET_N is active low and the active time should be no less than 5 ms.

3 Appendix: Schematics of Reference Design

UM680A Hardware Reference



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